What is claimed is:

1. A rearrangement sheet comprising an insulating sheet and conductive metallic patterns formed on this insulating sheet.

2. The rearrangement sheet according to claim 1, wherein said conductive metallic patterns comprise electrodes for wire bonding with external electrodes.

3. The rearrangement sheet according to claim 1, wherein said conductive metallic patterns are metallic wiring patterns.

4. The rearrangement sheet according to claim 1, wherein said conductive metallic patterns are conductive metal plated patterns.

5. The rearrangement sheet according to claim 4, wherein said conductive metallic patterns comprise a laminated pattern of an underlying plated pattern formed on the upper surface of the insulating sheet and a conductive metal plated pattern formed on this underlying plated pattern.

6. The rearrangement sheet according to claim 1, wherein an element mounting region is provided in a region on said insulating sheet other than the region where said conductive metallic patterns are formed, and an insulating adhesive sheet is provided in this element mounting region.

7. The rearrangement sheet according to claim 1, wherein said insulating sheet is an insulating adhesive sheet.

8. A semiconductor device comprising:

a substrate;

a first element provided with a plurality of first bonding pads formed on the upper surface of this substrate;

a second element provided with a plurality of second bonding pads formed on the upper side of this first element;

a plurality of bonding posts provided in a region of the upper surface of said substrate other than the first element formation region;

first wires that connect post for first pad connection, of the bonding posts, and first pads for bonding post connection, of said first bonding pads;

wherein a rearrangement sheet provided with an insulating sheet and a plurality of conductive metallic patterns that are formed on this insulating sheet is provided between said first element and said second element;

said conductive metallic patterns are formed in a region, which is a region on said insulating sheet exposed from said second element, comprising a first position that can be reached by the straight line extending from a post for second pad connection, of said bonding posts, without contacting said first bonding pads, and a second position, capable of wire bonding with the second pads for bonding post connection, of said second bonding pads;

these conductive metallic patterns and said post for second pad connection are connected by first relay wires; and

said conductive metallic patterns and said second pads for bonding post connection are connected by second relay wires.

9. The semiconductor device according to claim 8, wherein said conductive metallic patterns are constituted by an underlying plated pattern formed on the upper surface of said insulating sheet and a conductive metal plated pattern formed on this underlying plated pattern.

10. The semiconductor device according to claim 8, wherein said conductive metallic patterns are metallic wiring patterns formed on the upper surface of said insulating sheet.

11. The semiconductor device according to claim 8, wherein said conductive metallic patterns comprise a metallic wiring pattern formed on the upper surface of said insulating sheet and conductive metal plated patterns provided on these metallic wiring patterns in a region including said first position and in a region including said second position separately or continuously.

12. A semiconductor device comprising:

a semiconductor element having a plurality of bonding pads formed on the upper surface thereof;

a rearrangement sheet comprising an insulating sheet and conductive metallic patterns electrically connected with said bonding pads, stuck onto a region of this semiconductor element other than the region where the bonding pads are formed; and

a sealed portion that seals the upper surface of said semiconductor element so as to cover said rearrangement sheet;

wherein said conductive metallic patterns comprise rearrangement posts of the same number as said bonding pads,

wire connection portions of the same number as the bonding pads, and rewiring leads that connect said rearrangement posts and said wire connection portions;

said wire connection portions and said bonding pads are connected by metallic wires,

conductive posts are formed on the upper surface of said rearrangement posts; and

part of these conductive posts is exposed from said sealed portion.

13. The semiconductor device according to claim 12, wherein said conductive metallic patterns are conductive metallic wiring patterns.

14. The semiconductor device according to claim 12, wherein said conductive metallic patterns are conductive metal plated patterns.

15. The semiconductor device according to claim 12, wherein, of said conductive metallic patterns, said rearrangement posts and said rewiring leads are constituted by conductive metallic wiring patterns; and

said wire connection portions are constituted by conductive metallic wiring patterns and conductive metal plated patterns formed on these conductive metallic wiring patterns.

16. A method of manufacturing a rearrangement sheet comprising:

a step of providing on an insulating film a plurality of masks corresponding to the shape of conductive metallic patterns in single chip units;

a step of forming a plurality of conductive metal plated patterns in single chip units on said insulating film using said plurality of masks;

a step of removing said masks; and

a step of forming a plurality of insulating sheets provided with conductive metal plated patterns in single chip units, by dividing the insulating film formed with said plurality of conductive metal plated patterns in single chip units, into each single chip unit.

17. The method of manufacturing a rearrangement sheet according to claim 16, further comprising a step of, after the step of removing said masks and before the step of dividing said insulating film, determining an element mounting region in a region on this insulating film other than the region where said conductive metal plated patterns are formed, and forming an insulating adhesive sheet on this element mounting region.

18. The method of manufacturing a rearrangement sheet according to claim 16, wherein said insulating film is an insulating adhesive film.

19. A method of manufacturing a semiconductor device comprising:

a step of sticking a rearrangement sheet provided with conductive metallic patterns onto a region at the upper

surface of a semiconductor element provided with a plurality of bonding pads and exposed from the bonding pads;

a step of connecting said bonding pads and wire connection portions of said conductive metallic patterns by fine metallic leads;

a step of forming conductive posts on rearrangement posts of said conductive metallic patterns by stud bumps produced by wire bonding;

a step of forming a sealed portion by sealing using molded resin so as to cover said bonding pads, said rearrangement sheets, said fine metallic leads and said conductive posts on the upper surface of said semiconductor element; and

a step of exposing the upper surfaces of said conductive posts by grinding the surface of said sealed portion.

20. The method of manufacturing a semiconductor device according to claim 19, wherein said semiconductor element is one element of a group of a plurality of semiconductor elements formed on a semiconductor wafer; and

wherein the processes from the step of sticking on said rearrangement sheet up to the step of grinding said sealed portion are performed simultaneously in respect of each of the semiconductor elements of said semiconductor element group, and then the sealed semiconductor wafer is divided into respective semiconductor elements.